CLAIMS

What is claimed is:

1. A class-AB output stage for an operational amplifier, comprising:

first and second differential input signal lines;

a first pair of complementary output transistors;

a current mirror including first and second current sources;

a first biased class-AB control circuit including a first pair of complementary control transistors, the first control circuit being connected in series between the first differential signal line and the first current source;

a second biased class-AB control circuit including a second pair of complementary control transistors, the second control circuit being connected in series between the second differential signal line and the second current source; and

a pair of differential amplifiers, each differential amplifier having first and second inputs and a current output, the respective outputs of the differential amplifiers being connected to a feedback signal line, the first inputs of the differential amplifiers being connected to respective gates of the first output transistors,

wherein the first control circuit is connected between the respective first inputs of the differential amplifiers and the second control circuit is connected between the respective second inputs of the differential amplifiers, and

wherein the feedback signal line is connected to the current mirror for reducing output conductance associated with the current mirror.

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2. The class-AB output stage of claim 1 wherein the first and second class-AB control circuits each include first and second complementary control transistors, and further including first and second bias generators, an output of the first bias generator being connected to respective gates of the first control transistors, and an output of the second bias generator being connected to respective gates of the second control transistors.

3. The class-AB output stage of claim 2 wherein each one of the first and second bias generators includes a current source connected in series with a plurality of diode-connected bias transistors.

4. The class-AB output stage of claim 2 wherein each one of the first and second bias generators includes first and second current sources and first and second bias transistors, the first current source being connected in series with the first bias transistor, the second current source being connected in series with the second bias transistor, a gate of the first bias transistor being connected between the second current source and the second bias transistor, a gate of the second bias transistor being connected between the first current source and the first bias transistor at the output of the respective bias generator, thereby improving quiescent current stability over power supply voltage of the class-AB output stage.

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5. The class-AB output stage of claim 1 further including a second pair of complementary output transistors, a source and a drain of a first one of the second output transistors being connected to a drain of a corresponding first one of the first output transistors, a gate of the first one of the second output transistors being connected to a source of a first one of the first control transistors, a source and a drain of a second one of the second output transistors being connected to a drain of a corresponding second one of the first output transistors, a gate of the second one of the second output transistors being connected to a source of a second one of the first control transistors, thereby reducing asymmetry caused by gate parasitic capacitance of the first output transistors.

6. The class-AB output stage of claim 5 further including a first resistive element coupled between the gate of the first one of the second output transistors and the source of the first one of the first control transistors, and a second resistive element coupled between the gate of the second one of the second output transistors and the source of the second one of the first control transistors.

7. The class-AB output stage of claim 1 wherein each transistor included therein is implemented in MOS technology.

8. The class-AB output stage of claim 1 wherein each transistor included therein is implemented in bipolar technology.

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9. A method of biasing a class-AB output stage for an operational amplifier, comprising the steps of:

providing first and second differential input signal lines;

connecting a pair of complementary output transistors;

connecting first and second current sources to form a current mirror;

connecting a first class-AB control circuit in series between the first differential signal line and the first current source, the first control circuit including a first pair of complementary control transistors;

connecting a second class-AB control circuit in series between the second differential signal line and the second current source, the second control circuit including a second pair of complementary control transistors;

connecting respective current outputs of a pair of differential amplifiers to a feedback signal line, each differential amplifier having first and second inputs, and connecting the first inputs of the differential amplifiers to respective gates of the output transistors;

connecting the first control circuit between the respective first inputs of the differential amplifiers, and connecting the second control circuit between the respective second inputs of the differential amplifiers;

connecting the feedback signal line to the current mirror to reduce output conductance associated with the current mirror; and

biasing the first and second control circuits by at least one bias generator.

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10. The method of claim 9 wherein the biasing step includes biasing the first and second control circuits by first and second bias generators, wherein the first and second control circuits each include first and second complementary control transistors, wherein an output of the first bias generator is connected to respective gates of the first control transistors, and an output of the second bias generator is connected to respective gates of the second control transistors.

11. The method of claim 10 wherein each one of the first and second bias generators includes a current source connected in series with a plurality of diode-connected bias transistors.

12. The method of claim 10 wherein each one of the first and second bias generators includes first and second current sources and first and second bias transistors, the first current source being connected in series with the first bias transistor, the second current source being connected in series with the second bias transistor, a gate of the first bias transistor being connected between the second current source and the second bias transistor, a gate of the second bias transistor being connected between the first current source and the first bias transistor at the output of the respective bias generator, thereby improving quiescent current stability over power supply voltage of the class-AB output stage.

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13. The method of claim 9 wherein each transistor included in the output stage is implemented in MOS technology.

14. The method of claim 9 wherein each transistor included in the output stage is implemented in bipolar technology.

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